[Document Name] Specification

[Title of the Invention]

photo-diode Array, a method of making thereof, a semiconductor device and a radiation detector

[Claims]

[Claim 1] A photodiode array comprising a semiconductor substrate made of a first conductive type semiconductor, wherein a plurality of photodiodes are formed at opposite side of an light incident surface of the substrate, wherein a plurality of recessed portions are formed like an array at the opposite side of the incident surface of the light to be detected, and wherein said photodiodes are formed like an array by forming a second conductive type semiconductor region consist of the second conductive type semiconductor is formed at the bottoms of the recessed portions.

[Claim 2] A photodiode array according to claim 1, wherein a first conductive type accumulation layer having higher impurity concentration than that of the semiconductor substrate is provided at the incident surface of the semiconductor substrate.

[Claim 3] A photodiode array according to claim 1, wherein said recessed portion is surrounded by a frame thicker than the bottom of said semiconductor substrate, and wherein a first conductive type separation layer having higher concentration than that of said semiconductor substrate is formed at said frame.

[Claim 4] A photodiode array according to claim 3, wherein a electrode pad is provided via an electric insulating layer at said frame, and wherein conductive member that electrically connects said second conductive type semiconductor region and said electrode pad is provided.

[Claim 5] A photodiode array according to claim 4, wherein said conductive member is formed on an electrically insulating layer that is formed at the opposite side of said semiconductor substrate, wherein one end thereof is connected to said second conductive type semiconductor region via a

contact hole formed at said electric insulating layer, and wherein the other end thereof is connected to said electrode pad.

[Claim 6] A photodiode array according to claim 3, wherein said second conductive type semiconductor region extends to the boundary portion between said recessed portion and said frame from said bottom.

[Claim 7] A photodiode array according to claim 6, said frame has a conductive member electrically connected to a portion extending to the boundary portion between said recessed portion and said frame at said second conductive type semiconductor region, and an electrode pad electrically connecting to said conductive member.

[Claim 8] A photodiode array according to claim 6, wherein said second conductive type semiconductor region reaches to a part of said frame.

[Claim 9] A photodiode array according to claim 1, wherein the opening size of said recessed portion tapers toward said incident surface from said opposite surface.

[Claim 10] A photodiode array according to claim 1, wherein said semiconductor substrate has an etching stop layer at a predetermined depth from said opposite surface, and wherein said recessed portion is formed by etching said semiconductor substrate from said opposite surface to at least said etching stop layer.

[Claim 11] A photodiode array according to claim 1, wherein said semiconductor substrate has an insulating layer at a predetermined depth from said opposite surface, and wherein said recessed portion is formed by etching said semiconductor substrate from said opposite surface to at least an exposed surface of said insulating film.

[Claim 12] A photodiode array according to claim 1, wherein the crystal orientation in the incident surface side and the crystal orientation in the opposite side surface of the said semiconductor substrate crosses at the predetermined depth from said opposite surface, and wherein said recessed portion

is formed by etching said semiconductor substrate from said opposite surface to said at least to the exposed surface that provides the crystal orientation crossing surface.

[Claim 13] A method of manufacturing a photodiode array, comprising:

a step of forming a plurality of recessed portions arranged like array by thinning an opposite surface of a first conductive type semiconductor substrate, the opposite surface is opposite to the incident surface of the light to be detected;

a step of forming a second conductive type semiconductor region at the bottom of said recessed portion.

[Claim 14] A method of manufacturing a photodiode array according to claim 13, further comprising a step of forming a first conductive type accumulation layer at the incident surface side having higher impurity concentration than that of said semiconductor substrate.

[Claim 15] A method of manufacturing a photodiode array comprising:

a step of preparing a first conductive type first semiconductor substrate and a first conductive type second semiconductor substrate that has a different crystal orientation from that of said first semiconductor substrate and that has faster etching rate than that of said first semiconductor substrate, and bonding said second semiconductor substrate to the opposite surface side to the incident surface of light to be detected of said first semiconductor substrate;

a step of forming a plurality of recessed portions arranged like an array by etching said second semiconductor substrate until at least the opposite surface of said first semiconductor substrate is exposed; and

a step of forming a second conductive type semiconductor region at the bottom of said recessed portion.

[Claim16] A method of manufacturing a photodiode array according to claim 15, further comprising the step of forming a first conductive type accumulation layer having higher concentration than that of said first semiconductor substrate

at the incident surface of said first semiconductor substrate.

[Claim 17] A method of manufacturing a photodiode array, comprising:

a step of preparing a first conductive type first semiconductor substrate and a first conductive type second semiconductor substrate, and bonding said second semiconductor substrate to the opposite surface to the incident surface of the light to be detected of said first semiconductor substrate via an etching stop layer;

a step of forming a plurality of recessed portions arranged like an array by etching said second semiconductor substrate until at least said etching stop layer is exposed; and

a step of forming a second conductive type semiconductor region at the bottom of said recessed portion.

[Claim 18] A method of manufacturing a photodiode array according to claim 17, further comprising the step of forming a first conductive type accumulation layer having higher impurity concentration than that of said first semiconductor substrate at the incident surface of said first semiconductor substrate.

[Claim 19] A method of manufacturing a photodiode array, comprising:

a step of preparing a first conductive type first semiconductor substrate and a first conductive type second semiconductor substrate, and bonding said second semiconductor substrate to the opposite surface to the incident surface of the light to be detected of said first semiconductor substrate via a insulating film;

a step of etching said second semiconductor substrate until at least said insulating film is exposed to form a plurality of recessed portions arranged like an array; and

a step of forming a second conductive type semiconductor region at the bottom of said recessed portion.

[Claim 20] A method of manufacturing a photodiode array according to claim 19, further comprising the steps of forming

a first conductive type accumulation layer having higher concentration than said first semiconductor substrate at the incident surface of said first semiconductor substrate.

[Claim 21] A method of manufacturing a photodiode array, comprising:

a step of preparing a first conductive type first semiconductor substrate with a plurality of the second conductive type semiconductor regions arranged like an array that is formed at the opposite surface to the incident surface of light to be detected;

a step of bonding a first conductive type second semiconductor substrate to said opposite surface;

a step of exposing said second conductive type semiconductor region by etching regions corresponding to said second conductive type semiconductor regions in said second semiconductor substrate.

[Claim 22] A method of manufacturing a photodiode array according to claim 21, further comprising the step of forming a first conductive type accumulation layer having higher impurity concentration than that of said first semiconductor region at the incident surface of said first semiconductor substrate.

[Claim 23] A method of manufacturing a photodiode array according to claim 21, wherein said first semiconductor substrate and said second semiconductor substrate are bonded so as to cross the crystal orientations thereof, in the bonding step of said second semiconductor substrate.

[Claim 24] A method of manufacturing a photodiode array according to claim 21, wherein an etching stop layer is provided between said first semiconductor substrate and said second semiconductor substrate in the bonding step of said second semiconductor substrate.

[Claim 25] A method of manufacturing a photodiode array according to claim 21, wherein an insulating film is provided between said first semiconductor substrate and said second semiconductor substrate in the bonding step of said second

semiconductor substrate.

[Claim 26] A radiation detector comprising:

a photodiode array recited in one of claim 1 to claim 21, and

a scintillator that illuminates in response to the incidence of a radiation, arranged at the incident surface of said semiconductor substrate.

[Claim 27] A radiation detector comprising:

a photodiode array recited in one of claim 3 to claim 8;

a scintillator that illuminates in response to the incidence of a radiation, arranged at the incident surface of said semiconductor substrate; and

a substrate supporting said photodiode array;

wherein said substrate is electrically connected to said photodiode array via an electrode pad formed on said frame.

[Claim 28] A radiation detector according to claim 27, wherein a resin is filled in a space between said substrate and said opposite surface of said semiconductor substrate.

[Claim 29] A semiconductor device comprising:

a photodiode array recited in one of claim 3 to claim 8,

a substrate supporting said photodiode array,

wherein said substrate is electrically connected to said photodiode array via an electrode pad provided on said frame.

[Claim 30] A semiconductor device according to claim 29, wherein a resin is filled in a space between said substrate and said opposite surface of said semiconductor substrate.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Pertains]

The present invention relates to a photodiode array, and the manufacturing method thereof, a semiconductor device comprising the photodiode array, and a radiation detector comprising the photodiode array.

[0002]

[Prior art]

In the implementation of a photodiode array for CT, a three

dimensional implementation is necessary. In the three dimensional implementation, it is necessary that outputting signal from the opposite surface to the incident surface of the light to be detected, and therefore, a back illuminated photodiode array is used in general.

[0003]

In the back illuminated photodiode array, when the distance between the pn junction and the light incident surface is large, carriers generated in the substrate cannot be derived as a signal because of the recombination in the carrier movement to the pn junction. Therefore, it is necessary to minimize the distance between the pn junction and the light incident surface by all possible means..

[0004]

A back illuminated photodiode array shown in fig. 25 is known as an example of shortening this distance (for example, see patent reference 1. In the back illuminated photodiode array, an a p-type diffusion layer 106 is formed in the n-type layer 103 from one side of the substrate.

[0005

[patent reference 1]

Japanese patent laid-open application No. 7-333348

[0006]

[Problem to be Solved by the Invention]

However, since the p-type diffusion layer 105 is formed by implanting an impurity, it is difficult to form the p-type impurity layer 106 with uniform thickness enough to obtain sufficient sensitivity. There is an disadvantage that manufacturing the above photodiode array is difficult.

[0007]

The invention has been carried out in consideration of the problems and to provide a back illuminated photodiode array that can be manufactured easily while a high detection sensitivity is maintained, the manufacturing method thereof, a semiconductor device and a radiation detector.

[0008]

[Means for Solving the Problem]

The photodiode array of the present invention comprises a semiconductor substrate made of a first conductive type semiconductor, wherein a plurality of photodiodes are formed at opposite side of an light incident surface of the substrate, wherein a plurality of recessed portions are formed like an array at the opposite side of the incident surface of the light to be detected, and wherein said photodiodes are formed like an array by forming a second conductive type semiconductor region consist of the second conductive type semiconductor is formed at the bottoms of the recessed portions.

[0009]

In the photodiode array according to the present invention, since the second conductive type semiconductor region is provided at the bottom of the recessed portion formed on the opposite surface, the distance between the incident surface and the second conductive type semiconductor region of the photodiode can be shortened. Therefore, the carrier recombination in their movement is suppressed, the carriers being generated in response to the incidence of light to be detected, and the sensitivity of the photodiode array can be maintained high.

[0010]

Further, since the thickness of the second conductive type semiconductor region can be thinner than that of the prior art, the second conductive type semiconductor region can be formed easily by using thermal diffusion of the second conductive type impurity or the like to form a photodiode array easier than that in the conventional technique.

[0011]

Further, since a plurality of recessed portions are formed in an array arrangement at the opposite surface of the semiconductor substrate, each of the recessed portions are surrounded by a semiconductor substrate(frame) having a thickness than that of the recessed portion of the semiconductor substrate. This frame makes the mechanical strength of the

photodiode array enough high from a practical standpoint.

[0012]

Further, a first conductive type accumulation layer is preferably provided at the incident surface of the semiconductor substrate, the layer having higher impurity concentration than that of the semiconductor substrate. When using this structure, a trap of the signal carriers at the surface or the interface of the AR coating is suppressed, the carriers being generated at and near the incident surface in response to the incidence of the light (especially short wavelength light) to be detected on the surface of the semiconductor substrate. Therefore, the sensitivity of the photodiode array can be maintained high.

[0013]

Further, the recessed portion is surrounded by the frame consist of the semiconductor substrate, the frame having thickness thicker than the recessed portion, and the frame preferably has a first conductive type separation layer having higher impurity concentration than the semiconductor substrate. In this structure, the photodiodes respectively formed at the recessed portions are electrically separated, and cross-talk between the photodiodes will be decreased.

[0014]

Further, an electrode pad is preferably provided at the frame via an electrical insulating layer, and a conductive member that electrically connects the second conductive type semiconductor region and electrode pad is preferably provided. In this structure, it is not necessary to form electrode pads on the recessed portion that has low mechanical strength, and the bottom of the recessed portion can be protected by the mechanical damage.

[0015]

Further, the conductive member is preferably formed on the electrical insulating layer that is formed on the opposite side of the semiconductor substrate, and the one end thereof is electrically connected to the second conductive type

semiconductor region via a contact hole formed at the electrical insulating layer and the other end thereof is electrically connected to the electrode pad. In this structure, the signal from the photodiode is conducted to the electrode pad by the conductive member (for example aluminum wiring or the like) from the second conductive type semiconductor region, and outputs from the electrode pad.

[0016]

Further, the second conductive type semiconductor region preferably extends to the boundary portion between the recessed portion and the frame from the bottom of the recessed portion. In this structure, the area that the second conductive type semiconductor region is provided can be greater than the area obtained when the second conductive type semiconductor region is only provided at the bottom of the recessed portion, then the area of receiving the carriers generated in the semiconductor substrate in response to the incidence of light to be detected. Therefore, the sensitivity of the photodiode can be high. Further, the second conductive type semiconductor region extends to the boundary portion (edge portion) between the recessed portion and the frame. The frame is easily stressed by the etching process, and the protruded frame easily receives an mechanical damage when the implementation, therefore, it will be a source of undesired carriers. The second conductive type semiconductor region is provided so as to extends this boundary portion, and the undesired carriers will be trapped in the second conductive type semiconductor region.

[0017]

Further, the frame preferably has a conductive member electrically connected to a portion extending to the boundary portion between the recessed portion and the frame at the second conductive type semiconductor region, and an electrode pad electrically connecting to the conductive member. In this structure, since the conductive member that connects the electrode pad and the second conductive type semiconductor

region may be merely provided on the frame, the recessed portion that has a low mechanical strength can be protected and the process of forming the conductive member will be easy.

[0018]

Further, the second conductive type semiconductor region preferably reaches to a part of the frame. In this structure, on the top of the frame, the second conductive type semiconductor region and the electrode pad can be electrically connected, therefore, forming a wiring on the bottom or the side wall of the recessed portion will be unnecessary, and it can merely be formed on the frame and the wiring forming process will be easy.

[0019]

Further, the opening size of the recessed portion preferably tapers toward the incident surface from the opposite surface. In this structure, since the recessed portion has a slope side, forming the second conductive type semiconductor region on the side wall of the recessed portion or forming a conductive member will be easy.

[0020]

Further, the semiconductor substrate has preferably an etching stop layer at a predetermined depth from the opposite surface, and wherein the recessed portion is formed by etching the semiconductor substrate from the opposite surface to at least the etching stop layer. In this structure, since the etching will be terminated at the etching stop layer when forming the recessed portion, the depth of the recessed portion will be controlled easy.

[0021]

Further, the semiconductor substrate has preferably an insulating layer at a predetermined depth from the opposite surface, and wherein the recessed portion is formed by etching the semiconductor substrate from the opposite surface to at least an exposed surface of the insulating film. In this structure, since the etching will be terminated at the insulating layer when forming the recessed portion, the depth

of the recessed portion will be controlled easy.

[0022]

Further, the crystal orientation in the incident surface side and the crystal orientation in the opposite side surface of the semiconductor substrate preferably crosses at the predetermined depth from the opposite surface, and wherein the recessed portion is formed by etching the semiconductor substrate from the opposite surface to the at least to the exposed surface that provides the crystal orientation crossing surface. In this structure, since the etching will be terminated at the crystal orientation crossing surface when forming the recessed portion, the depth of the recessed portion will be controlled easy.

[0023]

The method of manufacturing a photodiode array of the present invention comprises a step of forming a plurality of recessed portions arranged like array by thinning an opposite surface of a first conductive type semiconductor substrate, the opposite surface is opposite to the incident surface of the light to be detected; and a step of forming a second conductive type semiconductor region at the bottom of the recessed portion.

[0024]

In the method of manufacturing a photodiode array of the present invention, a plurality of recessed portions are formed like array on the opposite surface t the incident surface of light to be detected, and the bottom of the recessed portion has a second conductive type semiconductor region thereon, and therefore, the photodiodes are formed. In this structure, the distance between the incident surface and the photodiode's second conductive type semiconductor region can be shorted. Since the movement distance of the carriers generated in the semiconductor substrate in response to the light incident, and the carrier recombination will be suppressed, the sensitivity of the photodiode array will be maintained high.

[0025]

Further, since the thickness of the second conductive

type semiconductor region can be smaller than that of conventional technique, the second conductive type semiconductor region may be formed by a thermal diffusion of the second conductive type impurity or the like, the photodiode will be manufactured easier than the conventional technique.

[0026]

Further, at the opposite side of the semiconductor substrate, a plurality of recessed portions are formed like array, and each of the recessed portions is surrounded by a frame having thickness thicker than the thickness of the bottom of the semiconductor substrate. This frame makes the mechanical strength of the photodiode array enough high from a practical standpoint.

[0027]

Further, the method of manufacturing a photodiode array preferably further comprises a step of forming a first conductive type accumulation layer at the incident surface side having higher impurity concentration than that of the semiconductor substrate. In this method, since incident surface of the semiconductor substrate has the first conductive type accumulation layer having higher impurity concentration than the semiconductor substrate, a trap of the signal carriers at the surface or the interface of the AR coating is suppressed, the carriers being generated at and near the incident surface in response to the incidence of the light (especially short wavelength light) to be detected on the surface of the semiconductor substrate. Therefore, the sensitivity of the photodiode array can be maintained high.

[0028]

A method of manufacturing a photodiode array comprises: a step of preparing a first conductive type first semiconductor substrate and a first conductive type second semiconductor substrate that has a different crystal orientation from that of the first semiconductor substrate and that has faster etching rate than that of the first semiconductor substrate, and bonding the second semiconductor substrate to the opposite surface side

to the incident surface of light to be detected of the first semiconductor substrate; a step of forming a plurality of recessed portions arranged like an array by etching the second semiconductor substrate until at least the opposite surface of the first semiconductor substrate is exposed; and a step of forming a second conductive type semiconductor region at the bottom of the recessed portion.

[0029]

In the method of manufacturing the photodiode array, the distance between the incident surface of the detectable light and the second conductive type semiconductor region, that is the surface on which the photodiode is formed is determined by the thickness of the first semiconductor substrate. Therefore, the movement distance of the carriers generated in the semiconductor substrate will be shortened by thinning the first semiconductor substrate, and the carrier recombination will be suppressed. Therefore, the sensitivity of the photodiode array can be maintained high.

Further, the first semiconductor substrate and the second semiconductor substrate are bonded and the second semiconductor substrate is etched until the opposite surface of the first semiconductor substrate is exposed. In this method, the second semiconductor substrate has a plurality of recessed portions formed like an array. Therefore, the second conductive type semiconductor region is surrounded by the frame of the second semiconductor substrate, and the mechanical strength of the photodiode array will be sufficient from a practical view point.

Further, since the thickness of the second conductive type semiconductor region can be smaller than that of the conventional technique, the second conductive type semiconductor region will be easily formed by the thermal diffusion of the second conductive type impurity or the like, and the photodiode array will be manufactured easier than the conventional technique.

[0030]

Further, the method of manufacturing a photodiode array

preferably further comprises the step of forming a first conductive type accumulation layer having higher concentration than that of the first semiconductor substrate at the incident surface of the first semiconductor substrate. In this method, since the incident surface of the semiconductor substrate has the first conductive type accumulation layer having higher impurity concentration than that of the semiconductor substrate, a trap of the signal carriers at the surface or the interface of the AR coating is suppressed, the carriers being generated at and near the incident surface in response to the incidence of the light (especially short wavelength light) to be detected on the surface of the semiconductor substrate. Therefore, the sensitivity of the photodiode array can be maintained high.

[0031]

The method of manufacturing a photodiode array of the present invention comprises: a step of preparing a first conductive type first semiconductor substrate and a first conductive type second semiconductor substrate, and bonding the second semiconductor substrate to the opposite surface to the incident surface of the light to be detected of the first semiconductor substrate via an etching stop layer; a step of forming a plurality of recessed portions arranged like an array by etching the second semiconductor substrate until at least the etching stop layer is exposed; and a step of forming a second conductive type semiconductor region at the bottom of the recessed portion.

[0032]

In the manufacturing method of the photodiode array according to the present invention, the distance between the incident surface of the detectable light and the second conductive type semiconductor region that is the surface on which the photodiode array is formed is determined by the thickness of the first semiconductor substrate. Therefore, the movement distance of the carriers generated in the semiconductor substrate will be shortened by thinning the first semiconductor substrate, and the carrier recombination will be

suppressed. Therefore, the detection sensitivity photodiode array will be maintained high. Further, the first semiconductor substrate and the second semiconductor substrate are bonded, and the second semiconductor substrate is etched until at least the etching stop layer is exposed. Therefore, the second semiconductor substrate has a plurality of recessed portions arranged like an array. Therefore, the second conductive type semiconductor region is surrounded by the frame of the second semiconductor substrate, and the mechanical strength of the photodiode array will be sufficient from a practical view point. Further, since the thickness of the second conductive type semiconductor region can be smaller than that of the conventional technique, the second conductive type semiconductor region can be easily formed by a thermal diffusion of the second conductive type impurity or the like, and the photodiode array can be formed easier than the conventional method.

[0033]

Further, the method of manufacturing a photodiode array preferably further comprises the step of forming a first conductive type accumulation layer having higher impurity concentration than that of the first semiconductor substrate at the incident surface of the first semiconductor substrate. In this method, at the incident surface of the semiconductor substrate, since the first conductive type accumulation layer is provided having higher impurity concentration than that of the semiconductor substrate, a trap of the signal carriers at the surface or the interface of the AR coating is suppressed, the carriers being generated at and near the incident surface in response to the incidence of the light (especially short wavelength light) to be detected on the surface of the semiconductor substrate. Therefore, the sensitivity of the photodiode array can be maintained high.

[0034]

The method of manufacturing a photodiode array of the present invention comprises: a step of preparing a first

conductive type first semiconductor substrate and a first conductive type second semiconductor substrate, and bonding the second semiconductor substrate to the opposite surface to the incident surface of the light to be detected of the first semiconductor substrate via a insulating film; a step of etching the second semiconductor substrate until at least the insulating film is exposed to form a plurality of recessed portions arranged like an array; and a step of forming a second conductive type semiconductor region at the bottom of the recessed portion.

[0035]

In the manufacturing method of the photodiode array according to the present invention, the distance between the incident surface of the detectable light and the second conductive type semiconductor region, that is the surface on which the photodiode is formed is determined by the thickness of the first semiconductor substrate. Therefore, the movement distance of the carriers generated in the semiconductor substrate will be shortened by thinning the first semiconductor substrate, and the carrier recombination will be suppressed. Therefore, the sensitivity of the photodiode array can be maintained high.

Further, the first semiconductor substrate and the second semiconductor substrate are bonded, and the second semiconductor substrate is etched until at least the insulating film is exposed. In this method, the second semiconductor substrate has a plurality of recessed portions formed like an array. Therefore, the second conductive type semiconductor region is surrounded by the frame of the second semiconductor substrate and the mechanical strength of photodiode array becomes sufficient from a practical view point.

Further, since the second conductive type semiconductor region will be thinner than that of the conventional technique, the second conductive type semiconductor region can be easily formed by a thermal diffusion of the second conductive type impurity or the like, and the photodiode array can be formed

easier than the conventional method.

[0036]

Further, the method of manufacturing a photodiode array preferably further comprises the steps of forming a first conductive type accumulation layer having higher concentration than the first semiconductor substrate at the incident surface of the first semiconductor substrate. In this method, since the incident surface of the semiconductor substrate has the first conductive type accumulation layer having higher impurity concentration than that of the semiconductor substrate, a trap of the signal carriers at the surface or the interface of the AR coating is suppressed, the carriers being generated at and near the incident surface in response to the incidence of the light (especially short wavelength light) to be detected on the surface of the semiconductor substrate. Therefore, the sensitivity of the photodiode array can be maintained high.

[0037]

The method of manufacturing a photodiode array of the present invention comprises: a step of preparing a first conductive type first semiconductor substrate with a plurality of the second conductive type semiconductor regions arranged like an array that is formed at the opposite surface to the incident surface of light to be detected; a step of bonding a first conductive type second semiconductor substrate to the opposite surface; a step of exposing the second conductive type semiconductor region by etching regions corresponding to the second conductive type semiconductor regions in the second semiconductor substrate.

[0038]

In the method of manufacturing the photodiode array, the distance between the incident surface of the detectable light and the second conductive type semiconductor region, that is the surface on which the photodiode is formed is determined by the thickness of the first semiconductor substrate. Therefore, the movement distance of the carriers generated in the semiconductor substrate will be shortened by thinning the first

semiconductor substrate, and the carrier recombination will be suppressed. Therefore, the sensitivity of the photodiode array can be maintained high. Further, since the first semiconductor substrate itself does not have an enough mechanical strength of the photodiode array, the second semiconductor substrate is bonded to it and necessary and sufficient etching is performed in order to expose the second conductive type semiconductor region, and the second conductive type semiconductor region is surrounded by the frame of the second semiconductor substrate to sufficiently reinforce the mechanical strength of the photodiode array from a practical view point. Further, the thickness of the second conductive type semiconductor region can be thinner than that of the conventional art, the second conductive type semiconductor region is easily formed by the thermal diffusion of the second conductive impurity or the like, and the photodiode array can be easier than the conventional method.

[0039]

Further, the method of manufacturing a photodiode array preferably further comprises the step of forming a first conductive type accumulation layer having higher impurity concentration than that of the first semiconductor region at the incident surface of the first semiconductor substrate. In this method, since incident surface of the semiconductor substrate has the first conductive type accumulation layer having higher impurity concentration than the semiconductor substrate, a trap of the signal carriers at the surface or the interface of the AR coating is suppressed, the carriers being generated at and near the incident surface in response to the incidence of the light (especially short wavelength light) to be detected on the surface of the semiconductor substrate. Therefore, the sensitivity of the photodiode array can be maintained high.

[0040]

Further, the first semiconductor substrate and the second semiconductor substrate are preferably bonded so as to cross

the crystal orientations thereof, in the bonding step of the second semiconductor substrate. In this method, when etching the second semiconductor substrate to expose the second conductive type semiconductor region, the etching can be terminated at the bonding surface (crystal orientation crossing surface)of the first semiconductor substrate and the second semiconductor substrate, therefore, this process can be controlled easy.

[0041]

Further, an etching stop layer is preferably provided between the first semiconductor substrate and the second semiconductor substrate in the bonding step of the second semiconductor substrate. In this method, when the second semiconductor substrate is etched to expose the second conductive type semiconductor region, the etching can be terminated at the etching stop layer that is positioned between the first semiconductor substrate and the second semiconductor substrate, therefore, this process can be controlled easy.

[0042]

Further, an insulating film is preferably provided between the first semiconductor substrate and the second semiconductor substrate in the bonding step of the second semiconductor substrate. In this method, when the second semiconductor substrate is etched to expose the second conductive type semiconductor region, the etching can be terminated at the insulating film that is positioned between the first semiconductor substrate and the second semiconductor substrate, therefore, this process can be controlled easy.

[0043]

A radiation detector according to the present invention comprises: a photodiode array of the present invention, and a scintillator that illuminates in response to the incidence of a radiation, arranged at the incident surface of the semiconductor substrate.

[0044]

In the radiation detector of the present invention, since

the scintillator having higher mechanical strength than the semiconductor substrate is arranged at the incident surface side of the semiconductor substrate, the semiconductor substrate is mechanically reinforced. In this structure, the warpage or the stress of the semiconductor substrate is suppressed.

[0045]

The radiation detector of the present invention comprises: a photodiode array of the present invention; a scintillator that illuminates in response to the incidence of a radiation, arranged at the incident surface of the semiconductor substrate; and a substrate supporting the photodiode array; wherein the substrate is electrically connected to the photodiode array via an electrode pad formed on the frame.

[0046]

In the radiation detector according to the present invention, since the scintillator is arranged at the incident surface side of the semiconductor substrate, the semiconductor substrate is reinforced mechanically, the warpage of the stress of the semiconductor substrate is suppressed. Further, the photodiode array and the substrate are electrically connected by the electrode pad, the detection signal from the photodiode array can be derived via the substrate. Further, since the electrode pad is provided on the frame that has a good mechanical strength of the semiconductor substrate, when the photodiode array is implemented on the substrate, it is difficult to receive an mechanical damage for the semiconductor substrate. Further, when the space between the substrate and the other surface of the semiconductor substrate is an air layer, the adiathermancy between the substrate and the semiconductor substrate becomes good, and the thermal flowing from the substrate can be suppressed.

[0047]

Further, the space between the substrate and the opposite surface of the semiconductor substrate is preferably filled

with a resin. In this structure, since the opposite surface of the semiconductor substrate and the substrate are bonded by the resin, the mechanical strength ot the semiconductor substrate can be increased, and warpage or the stress of the semiconductor substrate can be suppressed.

[0048]

The semiconductor device according to the present invention comprise: a photodiode array of the present invention; and a substrate supporting the photodiode array, wherein the substrate is electrically connected to the photodiode array via an electrode pad provided on the frame.

[0049]

In the semiconductor device according to the present invention, since the photodiode array and the substrate are electrically connected via the electrode pad, the detection signal from the photodiode array can be derived via the substrate. Further, since the electrode pad is provided on the frame that has a good mechanical strength of the semiconductor substrate, when the photodiode array is implemented on the substrate, it is difficult to receive the mechanical damage for the semiconductor substrate. Further, when the space between the substrate and the opposite surface of the semiconductor substrate is an air layer, adiathermancy of the substrate and the semiconductor substrate becomes good, and the thermal flowing from the substrate to the semiconductor substrate is suppressed.

[0050]

Further, the space between the substrate and the opposite surface of the semiconductor substrate is preferably filled with a resin. In this structure, since the opposite surface of the semiconductor substrate and the substrate are bonded by the resin, the mechanical strength of the semiconductor substrate can be increased, and the warpage or the stress of the semiconductor substrate can be suppressed.

[0051]

[Embodiments of the Invention]

The following is an explanation of the embodiments of the present invention. In the following drawings, the same symbols will be provided for the same elements and overlapping description will be omitted.

[0052]

(First embodiment)

Fig. 1 is a plan view showing the back illuminated photodiode array 1 according to the first embodiment, and Fig. 2 shows a schematic II-II cross sectional view of Fig. 1. In the following explanation, in n-type silicon substrate 3, the surface on which the pn junction is formed is called a surface and the surface on which the light to be detected L in incident is called back surface.

[0053]

Fig. 1 shows a plan view of the photodiode array 1 when viewed from the surface side (the opposite side to the incident surface of the light L to be detected. A plurality of recessed portions 4 are orderly formed like an array on the n-type silicon substrate 3 and Fig. 2 shows pn junction 2 formed at the bottom 4a of the recessed portion 4. In this structure, each of the recessed portions 4 forms a photodiode, and these photodiodes are arranged like an array to form a photodiode array 1

[0054]

The photodiode array 1 has n-type silicon substrate 3 having about 100～350μm thickness and impurity concentration of about 1×10^{12}～$1\times10^{15}/cm^3$ n-type silicon substrate 3. This n-type silicon substrate 3 has accumulation layer 8 at its back side formed by n-type impurity diffusion. The n-type impurity concentration in the accumulation layer 8 is in the range of 1×10^{15}～$1\times10^{20}/cm^3$, and set to be higher than the impurity concentration in n-type silicon substrate 3. Further, the accumulation layer 8 should have a thickness that does not overlap the p-type impurity diffusion region 5 formed on the surface of the n-type silicon substrate 3, and it is for example set to about 0.1～several μm.

[0055]

Further, on the back side of the n-type silicon substrate 3, AR film that suppresses the reflection of the incident detectable light L. The material of the AR film 9 can be selected from a SiO_2 film or a SiN_x film itself or the stack of these films.

[0056]

On the surface of the n-type silicon substrate 3, a plurality of recessed portions 4 is formed like an array. This recessed portion 4 has for example, at surface side, about 1mm×1mm size and its opening tapers towards the back side from the surface side. In this structure, the recessed portion 4 has a slope side surface 4b, and the second conductive type semiconductor region 5 or a conductive member is easily formed on the side 4b of the recessed portion 4.

[0057]

The depth of the recessed portion 4 is over 2μm, and the interval to the neighboring recessed portion 4 is for example 1.5mm. The bottoms 4a of these recessed portions 4 has a p^+-type impurity diffusion region 5, and the interface between the p+-type impurity diffusion region 5 and then-type silicon substrate 3 forms a pn junction 2. This p+-type impurity diffusion region 5 has an impurity concentration of about 1×10^{15} $\sim1\times10^{20}/cm^3$. This p+-type impurity diffusion region 5 and n-type silicon substrate 3 forms a photodiode. The distance between the back surface on which the light L to be detected in incident and the pn junction provided at the bottom 4a of the recessed portion 4 is about 10～100μm.

[0058]

The periphery of the arrayed recessed portion 4 is surrounded by a larger thickness frame than that of the n-type silicon substrate 3 at the bottom 4a of the recessed portion 4, and the frame6 has an n^+-type separation layer 7 that separates the photodiodes. The separation layer 7 has an impurity concentration of about $1\times10^{15}\sim1\times10^{20}/cm^3$, and the separation layer 7 has a depth of for example about 1 to several μm. Further, When the depth of the separation layer 7 becomes

large to electrically connect the accumulation layer 8 to it, the function of the PIN photodiode becomes superior in the uniform diffusion of the depletion layer.

[0059]

Further, the surface of the n-type silicon substrate 3 is covered with an insulating film, SiO_2 film 10. The frame 6 has an electrode pad 13 that outputs signal from the photodiode, it is electrically insulated from the n-type silicon substrate 3, that is, is provided via the SiO_2 film 10. This electrode pad 13 is consist of under bump metal (called UMB hereinafter) 13a and bump electrode13b. Further, the conductive member, aluminum wiring 12 electrically connects the p+-type impurity diffusion region 5 and the electrode pad and the electrode pad 13. The aluminum wiring 12 is formed on SiO_2 film 10 provided on the surface of the n-type silicon substrate 3, and it is electrically insulated from n-type silicon substrate 3 in the passage between the p+-type impurity diffusion region 5 and the electrode pad 13. Further, not shown in the figure, the electrode of the n-type silicon substrate 3 is similarly formed on the frame.

[0060]

Further, at the SiO_2 film 10 covering the bottom 4a of the recessed portion 4, a contact hole 11 that extends to the p^+-type impurity diffusion region 5 is formed, the one end of the aluminum wiring 12 is electrically connected to the p^+-type impurity diffusion region 5 via the contact hole 11. The aluminum wiring 12 extends to the SiO_2 film 10 covering the bottom 4a and the side 4b of the recessed portion 4 and the other end thereof is electrically connected to the electrode pad 13.

[0061]

Further, except for the region that the electrode pad 13 is formed, a passivation film 14 is formed on the n-type silicon substrate 3, the film being formed of SiO_2, SiN_x, polyimide, acrylate , or epoxy.

[0062]

As stated above, in the photodiode array 1 of the first

embodiment, since p+-type impurity diffusion region 5 is provided at the bottom 4a of the recessed portion 4 formed on the surface, the distance between the back surface of the n-type silicon substrate 3 on which the light L to be detected is incident and the pn junction of the photodiode can be shortened(for example 10～100μm). Therefore, the carrier recombination in the carrier movement can be suppressed, the carrier being generated in response to the light L to be detected is incident on it, and the detection sensitivity of the photodiode array 1 will be maintained high.

[0063]

Further, since the thickness of the p_+-type impurity diffusion region 5 can be thinner than that in the conventional technique,、p+-type impurity diffusion region 5 can easily be formed by the p-type impurity diffusion or the like, the photodiode array 1 can be manufactured easier than the conventional method.

[0064]

Further, on the surface of the semiconductor substrate, a plurality of recessed portions 4 are formed like an array, and recessed portion 4 has a frame that has larger thickness than the n-type silicon substrate 3 at the bottom 4a of the recessed portion 4. The frame6 makes the mechanical strength of the photodiode array 1 high from a practical view point.

[0065]

Further, the accumulation layer 8 suppresses the trap of carriers by the surface or the interface of AR coating , the carriers being generated near the back surface in response to the incident of light L (especially short wavelength light) to be detected on the n-type silicon substrate 3 from the back surface side. Therefore, carriers are effectively transmitted to the pn junction 2, and the detection sensitivity of the photodiode array1 can be maintained high. Even when the accumulation layer 8 is not provided, the photodiode array 1 has enough detection sensitivity that is practically allowable.

[0066]

Further, when separation layer 7 is formed on the frame6, photodiodes respectively formed in the recessed portions 4 are electrically separated, the cross talk between the photodiodes can be reduced. Even when the separation layer 7 is not provided, the photodiode array 1 has enough detection sensitivity that is practically allowable.

[0067]

As a first modification of the first embodiment, the separation layer 7 can provided over the whole top surface 6b of the frame 6. In this structure, in the implementation, while frame 6 receives a mechanical stress via the electrode pad 13 and the boundary portion (edge portion hereinafter)between the frame 6 and recessed portion 4 can receives a stress in the etching process, and undesired carriers easily generate, the undesired carriers are trapped to suppress the dark current.

[0068]

Further, as the second modification of the first embodiment, as shown in Fig. 4, the separation layer 7 is provided over the whole top surface 6b and p^+-type impurity diffusion region 5 is provided by using the slope side 4b of the recessed portion 4, while the layer does not overlap the separation layer 7. In this structure, in the implementation, while frame 6 receives a mechanical stress via the electrode pad 13 and the edge portion hereinafter of frame 6 can receives a stress in the etching process, and undesired carriers easily generate, the undesired carriers are trapped to suppress the dark current. Further, since the area of the p+-type impurity diffusion region 5 can be expanded, the area of receiving the carriers generated in response to the incidence of light L to be detected becomes large, and therefore, the detection sensitivity of the photodiode can be high.

[0069]

Next, the manufacturing method of the photodiode array 1 of the first embodiment will be explained with referring to Fig. 2 and Figs. 5 to Fig. 9.

[0070]

First, first n-type silicon substrate 3a having the impurity concentration of about $1\times10^{12}\sim1\times10^{15}/cm^3$ and the thickness of about $10\sim200\mu m$ is prepared. Next, p-type impurity, boron or the like is diffused in the opposite surface to the surface that light L to be detected in incident on to form an arrayed p^+-type impurity diffusion region 5. By this way, the opposite surface to the surface that the light L to be detected is incident on has regions to be an arrayed pn junctions 2, that is, to be photodiodes.

[0071]

According to the manufacturing method of the present embodiment, since the thickness of the p+-type impurity diffusion region 5 can be thinner than that of the conventional technique, p+-type impurity diffusion region 5 can be formed by p-type impurity thermal diffusion, and the photodiode array 1 can be formed easier than the conventional method.

[0072]

Next, second n-type silicon substrate 3b having the impurity concentration identical to that of the first n-type silicon substrate 3a and the thickness of about $2\sim500\mu m$. Next, second n-type silicon substrate 3b is bonded to the surface of the first n-type silicon substrate 3a where the p+-type impurity diffusion region 5 in formed (see Fig. 5). By this way, n-type silicon substrate 3 of first n-type silicon substrate 3a and second n-type silicon substrate 3b is obtained (see Fig. 6). After the bonding of the n-type silicon substrate 3b, the thickness can be adjusted to a predetermined thickness by way of grinding or polishing.

[0073]

Next, in the second n-type silicon substrate 3b, the region corresponding to the p^+-type impurity diffusion region 5 is etched to expose the p^+-type impurity diffusion region 5, and recessed portion 4 is formed. That is, an etching mask (SiNx) is formed on the surface (the opposite surface to the surface on which the light L to be detected is incident) of the second n-type silicon substrate 3b by way of plasma CVD or LP-CVD

method or the like to eliminate the SiNx film corresponding to the p^+-type impurity diffusion region 5. Further, an anisotropic etching, an alkali etching by using KOH or TMAH or the like, is applied to the second n-type silicon substrate 3b to expose the p^+-type impurity diffusion region 5, and the etching mask (SiNx) is eliminated (see Fig. 7). By using this, in n-type silicon substrate 3, an arrayed recessed portion 4 whose each of the opening size tapers toward the back side from the surface side are formed. At each of the bottom 4a of the recessed portion 4, p^+-type impurity diffusion region 5 is exposed and the frame 6 is defined between the recessed portions 4.

[0074]

Next, the photodiodes are electrically separated by introducing n-type impurity like phosphorous or the like to the predetermined portion of the top surface 6b of the frame 6 by an ion implantation or the like to form the separation layers 7. Next, after a thin thermal oxidation film is formed, an accumulation layer 8 is formed over the whole surface (back surface) on which the light L to be detected is incident, by diffusing the n-type impurity such as arsenic or the like to the depth of 0.1 to several μm. After that, SiO_2 film 10 that becomes the surface protection layer is formed by thermal oxidation or CVD technique. Further, AR film 9 of SiO_2 film is formed on the back side of the n-type silicon substrate 3 (see Fig. 8).

[0075]

Next, a contact hole 11 is formed by eliminating a part of SiO_2 film 10 that is positioned on the bottom 4a of the recessed portion 4. Further, aluminum wiring 12 is formed on the SiO_2 film 10 that is provided on the surface. The aluminum wiring 12 is patterned so as to have one end being in contact with the p+-type impurity diffusion region 5 via the contact hole 11, and to extend to the top surface 6b of the frame 6 at the other end via the bottom 4a and side 4b of the recessed portion 4 (see fig. 9). Here, the conductive member is not

limited to the aluminum wiring 12, it may be a wiring made of conductive material, for example, a copper wiring or a gold wiring or the like.

[0076]

Next, a passivation film 14 is formed on the surface of the n-type silicon substrate 3. The passivation film 14 made of SiO_2 or SiN_x film formed by plasma CVD method, or polyimide, acrylate , epoxy or urethane or the mixture of these materials can be used.

[0077]

Next, the passivation film 14 is eliminated at the region where the electrode pad 13 of the frame 6 is formed to connect the electrode pad 13 to the aluminum wiring 12. That is, UMB 13a is formed on the aluminum wiring 12 that is formed on the top surface 6b of the frame6 to form the bump electrode 13b on the UMB 13a (see Fig. 2). By using these steps, the photodiode array 1 of the first embodiment is obtained.

[0078]

Note that the UMB13a is provided for improving the bonding property between the aluminum wiring 12 and the bump electrode 13b. When a solder is used as the electrode 13b, since the bonding property between the aluminum wiring 12 and the solder is bad, the aluminum wiring 12 and the bump electrode 13b are bonded by way of the UMB13a. The UBM 13a is formed by production of Ni-Au by the electroless plating method or also by production of Ti-Pt-Au or Cr-Au by the lift off method.

[0079]

Furthermore, the bump electrode 13b is obtained by the solder ball mounting method or printing method for forming solder at a site of the UBM 13a and effecting reflow. The bump electrode 13b includes conductive bumps including metals such as gold, nickel, copper and conductive resins, in addition to solder.

[0080]

As a modified example of the above stated photodiode array 1 manufacturing method, the first n-type silicon substrate 3a

and the second n-type silicon substrate 3b can be bonded so as to cross their crystal orientations. For example, the first n-type silicon substrate 3a having crystal plane (111) is prepared, and a second n-type silicon substrate 3b having crystal plane (100) or (110) is bonded to the first n-type silicon substrate 3a. In this case, when the second n-type silicon substrate 3b is etched by the alkali etching, since the etching rate of the (111) plane is quite slow compared to that of the (100) or (110) plane, the etching can be easily terminated at the time when the p^+-type impurity diffusion region 5 formed on the first n-type silicon substrate 3a is exposed.

[0081]

According to the first modified example, the recessed portions 4 are obtained by etching the surface of n-type silicon substrate 3 and the photodiode array 1 can be obtained by applying similar processes to it after that, while the crystal orientations of the front and back side surface of the n-type silicon substrate 3 crosses at the predetermined depth of the surface.

[0082]

As a second modified example of the manufacturing method of the photodiode array 1, an insulating layer (etching stop layer) such as SiO_2 or the like can be provided between the first n-type silicon substrate 3a and the second n-type silicon substrate 3b. For example, a second n-type silicon substrate 3b on which a SiO_2 film is formed is bonded to the surface of the first n-type silicon substrate 3a. In this case, the etching can be easily terminated because the SiO2 film is not alkali etched when the alkali etching is applied to the second n-type silicon substrate 3b.

[0083]

According to the second modified example, the recessed portions 4 are formed by etching the surface of n-type silicon substrate 3 and the photodiode array 1 can be obtained by applying similar processes to it after eliminating the SiO_2 film at the bottom 4a, while it has SiO2 film (etching stop layer)

at a predetermined depth.

[0084]

(second embodemnt)

Fig. 10 shows a cross sectional view of the photodiode array 20 according to the second embodiment. The difference between the photodiode array 20 of the second embodiment and the photodiode array 1 will be explained. The photodiode array 20 of the second embodiment differs from the first embodiment in that the p^+-type impurity diffusion region 5 extends to the edge portion 4b of the frame 6 via the bottom 4a of the recessed portion 4 and the side 4b by using the slope side 4b of the recessed portion 4. That is, in the photodiode array 20, the p^+-type impurity diffusion region 5 reaches to a part of the top surface 6b of the frame6.

[0085]

In the photodiode array 20, the surface is covered with SiO_2 film 10. The SiO_2 film 10 covering the p^+-type impurity diffusion region 5 that extending to the edge poriton 6a of the frame 6 has a contact hole 11 that extends to the p^+-type impurity diffusion region 5. The aluminum wiring 12 as the conductive member for outputting the signal from the photodiode is provided on the frame6 and electrically connected to the p^+-type impurity diffusion region 5 via the contact hole 11. The aluminum wiring 12 is arranged between the electrode pad 13 provided on the frame6 and the p^+-type impurity diffusion region 5.

[0086]

As stated above, in the photodiode array 20 of the second embodiment, since the p^+-type impurity diffusion region 5 is provided on the region that includes the bottom 4a of the recessed portion 4 formed at the surface, the distance between the back side of the n-type silicon substrate 3 on which the light L to be detected is incident and the pn junction 2 of the photodiode can be shortened. Therefore, the recombination of carriers in their movement can be suppressed, the carriers being generated in response to the incidence of light L to be detected, and the detection sensitivity will be maintained high.

[0087]

Further, since the thickness of the p^+-type impurity diffusion region 5 can be thinner than that of the conventional technique, the p^+-type impurity diffusion region 5 can be formed by the p-type impurity thermal diffusion, and the photodiode array 20 can be manufactured easier than the conventional method.

[0088]

Further, on the surface of the n-type silicon substrate 3, a plurality of recessed portions 4 are formed like an array, the recessed portion 4 comprises a frame that has larger thickness than that of the n-type silicon substrate at the bottom 4a of the recessed portion 4. The frame6 make the mechanical strength of the photodiode array 20 enough high from a practical view point.

[0089]

Further, the accumulation layer 8 suppresses the trap of carriers by the surface or the interface of AR coating, the carriers being generated near the back surface in response to the incidence of light L (especially short wavelength light) to be detected on the n-type silicon substrate 3 from the back surface side. Therefore, carriers are effectively transmitted to the pn junction 2, and the detection sensitivity of the photodiode array 20 can be maintained high. Even when the accumulation layer 8 is not provided, the photodiode array 1 has enough detection sensitivity that is practically allowable.

[0090]

Further, when the separation layer 7 in formed on the frame6, the photodiodes that is formed by the recessed portions 4 are electrically separated to reduce the cross talk between the photodiodes. Even when the separation layer 7 is not provided, the photodiode array 1 has enough detection sensitivity that is practically allowable.

[0091]

Further, since p^+-type impurity diffusion region 5 extends to the edge portion 6a of the frame 6 and formed on the

top surface 6b, the contact hole 11 can be provided on the top surface 6b of the frame 6. As a result, it is not necessary to form aluminum wiring 12 on the bottom 4a or the side wall 4b of the recessed portion 4, the wiring electrically connecting the p^+-type impurity diffusion region 5 and the electrode pad 13, and therefore, the process of the aluminum wiring 12 becomes easy because it is merely formed on the frame 6.

[0092]

Further, in the photodiode array 20, the p^+-type impurity diffusion region 5 extends to the edge portion 6a of the frame 6 which has a low mechanical strength. In the implementation, undesired carriers are generated by stresses, the stress easily occurring in the edge portion of the frame 6 at the time of its etching process, or the mechanical stress occurring in the frame 6 via the electrode pad 13. However, in this structure, the undesired carriers are trapped to suppress the dark current.

[0093]

Further, as a modified example of the second embodiment, the etching depth will be controlled by bonding two substrates that the crystal orientations cross as shown in the first embodiment, by bonding two substrates via an etching stop layer, or by bonding two semiconductor substrate via an insulating film. Note that, although the semiconductor substrates having PN junction 2 are bonded in the first embodiment, the recessed portion 4 is formed by etching after both of the substrates are bonded in this modified example and the p+-type impurity diffusion region 5 is formed after that. This example differs in this point from that of the first embodiment.

[0094]

Next, the manufacturing method of the photodiode array 20 according to the second embodiment will be explained with referring to Fig. 10 and Figs. 11 to 18.

[0095]

First, the n-type silicon substrate 3 having the impurity concentration of about $1\times10^{12}\sim1\times10^{15}/cm^3$ and the thickness of about 300~600μm is prepared(see Fig. 11). Next, SiO_2 films

21a,21b are formed on the front and back side of the n-type silicon substrate 3 by a thermal oxidation or the like (see Fig. 12). Next, separation layer 7 that separates the photodiodes is formed at the front side of the n-type silicon substrate 3, and gettering layer 22 that getters the crystal defect of the n-type silicon substrate 3 is formed at the back side of the n-type silicon substrate.

[0096]

That is, at the front side of the n-type silicon substrate 3, an opening corresponding to the separation layer 7 is formed in the SiO_2 film 21a by the photo-etching process. Similarly, SiO_2 film 21b is eliminated at the back side of the n-type silicon substrate 3. After that, the separation layer 7 and gettering layer 22 having impurity concentration of about $1\times10^{15}\sim 1\times10^{20}/cm^3$ are formed by thermally diffusing phosphorous to the n-type silicon substrate 3 and thermal oxidized (see Fig. 13). Note that an diffusion wafer having n-type impurity concentration of about $1\times10^{15}\sim1\times10^{20}/cm^3$ can be used instead of forming the gettering layer 22.

[0097]

Next, p^+-type impurity diffusion region 24 that the p-type impurity such as boron is diffused is formed at the front surface of the n-type silicon substrate 3. This p+-type impurity diffusion region 24 neighbors the separation layer 7 by a predetermined distance. This p^+-type impurity diffusion region 24 is etched in the process of forming the recessed portion 4 that is performed after this process (see Fig. 16), and becomes the p^+-type impurity diffusion region 5 that positioned at the region including the edge portion 6a of the frame 6 to the side 4b of the recessed portion 4.

[0098]

Specific manufacturing process will be explained below. An opening is formed at the SiO_2 film 23a by a photo-etching process in the front side of the n-type silicon substrate 3, p-type impurity such as boron or the like is diffused to this via this opening, and after that, it is thermally oxidized. By

this processes, impurity diffusion layer 24 having impurity concentration of about $1\times10^{15}\sim1\times10^{20}/cm^3$ p^+-type will be formed (see Fig. 14).

[0099]

Next, the gettering layer 22 is eliminated by polishing the back side of the n-type silicon substrate 3. Further, SiN_x film 26a,26b are formed on the front and back side of the n-type silicon substrate 3 by LP-CVD method. After that, regions of SiNx film 26a and SiO_2 film 25a will be eliminated by an etching process, the region becoming the recessed portion 4 in the later process (see Fig. 15).

[0100]

Next, in the former process, the region that the SiN_x film 26a and SiO_2 film 25a are eliminated is anisotropic etched by an alkali etching process using KOH aqueous liquor to form the recessed portion 4 and the frame6. The anisotropic etching is performed until the depth reaches to at least more than 2μm. By using this way, the recessed portion 4 whose the opening size tapers toward to the back side from the front side is formed at the front side of the n-type silicon substrate 3.

[0101]

Then, p^+ type impurities such as boron are diffused around the bottom 4a and side surface 4b of the recessed portions 4 exposed by anisotropic etching and followed by thermal oxidation. This step yields the p^+-type impurity diffusion region 5 around the bottom 4a of the recessed portions 4 through the edge part 6a of the frame part 6 and side surface 4b of the recessed portions 4. Namely, this step provides a region that will be made into photodiodes (see Fig. 16). As described above, although the undesired carriers are easily generated at the frame 6 or at the edge portion of the frame 6 by the stress because the frame 6 and the edge portion easily receive mechanical stress in the implementation, since the p^+-type impurity diffusion region 5 extends to the edge portion 6a between the recessed portion 4 and the frame 6 from the bottom 4a, the undesired carriers are trapped to inhibit production of dark

current.

[0102]

Further, since the thickness of p+-type impurity diffusion region 5 can be thinner than that of the prior art, the p+-type impurity diffusion region 5 can be formed easily by using thermal diffusion of the p-type impurity or the like to form a photodiode array 20 easier than that in the conventional technique.

[0103]

Next, SiNx films 26a and 26b used as the etching mask are eliminated, a buffer oxidation film is formed at the back side of the n-type silicon substrate 3, and arsenic is ion implanted into it after that and it is thermally oxidized, then the accumulation layer 8 is formed. Here, the accumulation layer 8 has a thickness that does not overlap the p^+-type impurity diffusion region 5 which is provided at the front side of the n-type silicon substrate 3. Further, the SiO2 film formed by a thermal oxidation and on the back side of n-type silicon substrate 3 is once removed, AR film 9 is formed by thermally oxidize the back side again (see Fig. 17).

[0104]

Next, contact hole 11 reaching to the p+-type impurity diffusion region 5 is formed at the SiO2 film 27a that is on the top surface 6b of the frame6 and aluminum wiring 12 is pattern on the frame 6 (see Fig. 18). As stated above, according the manufacturing method of the present embodiment, since the p+-type impurity diffusion region 5 extends to the top surface 6b of the frame, the contact hole 11 can be formed on the frame 6. Therefore, since the contact hole 11 and or the aluminum wiring 12 can selectively be patterned on the frame 6, the photo-etching process of the bottom 4a or the side wall 4b of the recessed portion 4 becomes unnecessary, the process becomes easy. Further, the patterning to the recessed portion 4 that is thin and has low mechanical strength becomes unnecessary, therefore, the stress is reduced.

[0105]

Further, the passivation film 14 is formed except for the region where the UBM 13a is formed at the front of the n-type silicon substrate 3. UMB 13a is formed on the aluminum wiring 12 that frame 6 is provided, UMB 13a is formed on the aluminum wiring 12, and bump electrode 13b is formed on the UMB13a, therefore, the photodiode array 20 of the second embodiment is formed (see Fig. 10).

[0106]

As a modified example of manufacturing the photodiode array 20, a bonded silicon substrate as shown in the first embodiment can be used. 、By using this, the depth of the etching can be controlled easy as explained in the first embodiment basically. In the first embodiment, the semiconductor substrate having PN junction 2 are bonded. On the other hand, in this modified example, the recessed portion 4 is formed by etching after bonding of the substrates, and after that, p^+-type impurity diffusion region 5 is formed. This example differs in this point from the first embodiment. For example, a SOI(Silicon on insulator) wafer, a SOS(Silicon on silicon) wafer, a bonded silicon wafer whose crystal orientations are crossed, or a bonded silicon epitaxial wafer and silicon wafer can be used as the bonded substrate.

[0107]

(third embodiment)

Fig. 19 shows a schematic cross sectional view of the semiconductor device according to the third embodiment. The semiconductor device 30 is a device comprised of the photodiode array 20 of the second embodiment that is electrically connected to the mounted wiring board K. That is, in the semiconductor device 30, the mounted wiring board K is connected to the photodiode array 20 via the bump 13b provided on the frame 6 positioned at the front side of the n-type silicon substrate 3.

[0108]

Further, in the semiconductor device 30 of the third embodiment, the space S between the surface of the n-type

silicon substrate 3 and the mounted wiring board K is an air layer.

[0109]

The bump electrode 13b and the mounted wiring board 31is connected by flip-chip bonding, and a solder bump, a nickel bump, a gold bump, a copper bump or a conductive resin bump can be used as the bump electrode 13b used in this bonding.

[0110]

In the semiconductor device 30 according to the present embodiment, since the connection to the mounted wiring board K is performed by the bump electrode 13b that is provided on the frame 6 (thick portion) with good mechanical strength of the n-type silicon substrate 3, the n-type silicon substrate 3 is hard to receive a mechanical damage in the implementation process. By this way, the generation of undesired carriers based on a mechanical damage can be suppressed and a dark current will be suppressed.

[0111]

Further, since the space S is an air layer, the adiathermancy between the mounted wiring board K and the n-type silicon substrate 3 can be increased. In the semiconductor device 30, while a signal processing circuit 51 or the like may be provided on the surface that is not connected to the n-type silicon substrate 3 of the mounted wiring board K (see Fig. 24), thermal generated from the signal processing circuit 51 reaches to the p^+-type impurity diffusion region 5(photodiode) of the n-type silicon substrate 3 via the mounted wiring board K, and the S/N ratio of the photodiode becomes bad. In the present embodiment, since the space S is an air layer, the flow of thermal into the p+-type impurity diffusion region 5(photodiode) from the mounted wiring board K will be suppressed, and the S/N ratio of the photodiode will be improved to reduce the generation of the dark current.

[0112]

As a first modified example of the third embodiment of the semiconductor device 30, the space S between the mounted

wiring board K and the n-type silicon substrate 3 is filled with an under fill resin 32 such as epoxy, silicone, urethane, acrylic resin or the compound thereof as shown in Fig. 20. In this structure, since the n-type silicon substrate 3 is bonded to the mounted wiring board having higher mechanical strength, n-type silicon substrate 3 is mechanically reinforced to reduce generation of warpage or stress of the n-type silicon substrate 3. In place of a step where resin is filled after flip chip bonding, bonding may be carried out by means of anisotropic conductive film (ACF), anisotropic conductive paste (ACP) or non-conductive paste (NCP).

[0113]

Further, as a second modified example of the third embodiment of the semiconductor device 30, as shown in Fig. 21, only a connected part of the n-type semiconductor substrate 3 with the mounted wiring board K (connected part of the bump electrode 13b with the electrode pad 31 on the wiring board side) is covered with the under-fill resin 32, and the space S is constituted with air. In this structure, since the connected part between the n-type silicon substrate 3 and the mounted wiring board K is reinforced by the under fill resin 32, the strength of this connected part will be improved. Further, since the space S is filled with air, the flow of the thermal into the p+-type impurity diffusion region 5(photodiode) from the mounted wiring board K can be minmized. The bonding may be carried out by means of anisotropic conductive film (ACF), anisotropic conductive paste (ACP) or non-conductive paste (NCP).

[0114]

(fourth embodiment)

Fig. 22 shows a schematic cross sectional view of the radiation detector 40 according to the fourth embodiment. The radiation detector 40 comprises the photodiode array 20 in the second embodiment and a scintillator 41 that illuminates in response the incidence of radiation bonded to the back side of the array 20.

[0115]

The radiation detector 40 of the fourth embodiment 40 is obtained by for example bonding a scintillator 42 to the back side of a scintillator 41 by a coupling resin 42 having almost same refractive index of scintillator 41.

[0116]

Since the scintillator 41 has larger thickness than that of n-type silicon substrate 3 in general, it has a good mechanical strength, and bonding the n-type silicon substrate 3 to the scintillator 41 mechanically reinforces the n-type silicon substrate 3 to reduce the warpage or stress of the n-type silicon substrate. Further, when bonding the scintillator 41, since the back side of the n-type silicon substrate 3 is flat, coupling resin 42 can be coated easily, and it suppresses the introduction of bubbles or the like into the bonding surface when the scintillator 41 is bonded. Note that the radiation detector of the present embodiment will be obtained by growing scintillator 41 on the n-type silicon substrate 3.

[0117]

(the fifth embodiment)

Fig. 23 shows a schematic cross sectional view of the radiation detector 50 of the fifth embodiment. The radiation detector 50 comprises the photodiode array 20 of the photodiode array 20 of the second embodiment, and the scintillator 41 that illuminates in response to the incidence of radiation bonded to the back side of the array, and comprises mounted wiring board K that supports the photodiode array, wherein the mounted wiring board K is connected to the photodiode array 20 via the bump electrode 13b provided on the frame 6 positioned at the surface of the n-type silicon substrate 3.

[0118]

The scintillator 41 illuminates when the light L to be detected such as X-ray or the like is incident on it in the radiation detector 50 of the preset embodiment. The illuminated light is incident on the n-type silicon substrate 3 from its back side to generate carriers in the n-type silicon

substrate 3. The generated carriers can be detected by the photodiode formed between the p+-type impurity diffusion region 5 and the n-type silicon substrate 3. The detected signal is output to the implementation substrate K via the bump electrode 13b provided on the frame 6.

[0119]

In the radiation detector 50, the back side of the n-type silicon substrate 3 is bonded to the scintillator 41, it has a good mechanical strength. Further, since the space S between the mounted wiring board K and the n-type silicon substrate 3 is filled with air, the flow of the thermal into the p+-type impurity diffusion region 5(photodiode) from the mounted wiring board K is minimized.

As shown in the third embodiment, the space S may be filled with an under fill resin 32 (see Fig. 20), the connected part of the bump electrode 13b and the implementation substrate K may be covered with the under fill resin (see Fig. 21). In this case, the mechanical strength of the photodiode array 20 can be increased.

[0120]

(sixth embodiment)

Fig. 24 shows a schematic cross sectional view of the radiation detector 60 according to the sixth embodiment. The radiation detector 60 differs in that the signal processing circuit 51 and signal output part 52 are provided from the radiation detector 50 of the fifth embodiment.

[0121]

The signal processing circuit 51 is provided on the surface of the mounted wiring board K, wherein the surface is not connected to the n-type silicon substrate, and flip-chip bonded or wired to the mounted wiring board K. Further, the signal output part 52 may be a pin-type, lead frame, flexible wiring substrate or the like.

[0122]

Since in the radiation detector 60, the scintillator 41 is bonded to the back side of the n-type silicon substrate 3,

it has a good mechanical strength. Further, the space S between the mounted wiring board K and the n-type silicon substrate 3 is filled with air, the flow of the thermal generated in the signal processing circuit 51 into the p^+-type impurity diffusion region 5(photodiode) via the mounted wiring board K can be minimized.

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[0123]

[Effects of the Invention]

According to the present invention,

This invention can provide a photodiode array which can be easily manufactured, with a high detection sensibility maintained, the manufacturing method, semiconductor device and radiation detector.

[Brief Description of the Drawings]

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plan view showing the photodiode array according to the first embodiment.

Fig. 2 is a schematic view showing the configuration of cross section taken along line II-II of Fig. 1.

Fig. 3 is a schematic view showing the cross sectional configuration of the first modification example according to the first embodiment.

Fig. 4 is a schematic view showing the cross sectional configuration of the second modification example according to the first embodiment.

Fig. 5 is a flow sheet showing a manufacturing method for the photodiode array according to the first embodiment.

Fig. 6 is a flow sheet showing a manufacturing method for the photodiode array according to the first embodiment.

Fig. 7 is a flow sheet showing a manufacturing method for the photodiode array according to the first embodiment.

Fig. 8 is a flow sheet showing a manufacturing method for the photodiode array according to the first embodiment.

Fig. 9 is a flow sheet showing a manufacturing method for the photodiode array according to the first embodiment.

Fig. 10 is a schematic view showing the cross sectional configuration of the photodiode array according to the second embodiment.

Fig. 11 is a flow sheet showing a manufacturing method for the photodiode array according to the second embodiment.

Fig. 12 is a flow sheet showing a manufacturing method for the photodiode array according to the second embodiment.

Fig. 13 is a flow sheet showing a manufacturing method for the photodiode array according to the second embodiment.

Fig. 14 is a flow sheet showing a manufacturing method for the photodiode array according to the second embodiment.

Fig. 15 is a flow sheet showing a manufacturing method for the photodiode array according to the second embodiment.

Fig. 16 is a flow sheet showing a method for the photodiode array according to the second embodiment.

Fig. 17 is a flow sheet showing a manufacturing method for the photodiode array according to the second embodiment.

Fig. 18 is a flow sheet showing a manufacturing method for the photodiode array according to the second embodiment.

Fig. 19 is a schematic view showing the cross sectional configuration of the semiconductor device of the third embodiment.

Fig. 20 is a schematic view showing the cross sectional configuration of the first modification example of the semiconductor device of the third embodiment.

Fig. 21 is a schematic view showing the cross sectional configuration of the second modification example of the semiconductor device of the third embodiment.

Fig. 22 is a schematic view showing the cross sectional configuration of the radiation detector of the fourth embodiment.

Fig. 23 is a schematic view showing the cross sectional configuration of the radiation detector of the fifth embodiment.

Fig. 24 is a schematic view showing the cross sectional configuration of the radiation detector of the sixth

embodiment.

Fig. 25 is a schematic view of the cross sectional configuration of a conventional photodiode array.

[Explanation of Reference Numerals]

1、20、··· photodiode array、2···pn junction 3··· n-type silicon substrate, 3a··· first n-type silicon substrate, 3b··· second n-type silicon substrate、4···recessed portion, 4a···bottom, 4b···side wall, 5···p^{+-}type impurity diffusion region, 6··· frame, 6a···edge portion, 7···separation layer, 8··· accumulation layer 、9···AR film, 10···SiO_2film, 11···contact hole, 12···aluminum wiring,13···electrode pad, 13a···UMB、13b··· bump electrode、14···passivation film, 30···semiconductor apparatus, 40、50···radiation detector.